AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

implanting an electrically inactive first impurity over substantially one entire side of a semiconductor substrate, excluding a region below a gate electrode, to form an implanted layer on an upper portion of the gate electrode and a surface layer of the semiconductor substrate; and

carrying out a heat treatment by light on the one side of the semiconductor substrate implanted with the first impurity,

wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate.

2. (Currently Amended) The method according to claim 1, further comprising:

implanting an electrically active second impurity having a predetermined conduction type to the semiconductor substrate before the heat treatment is carried out; and

carrying out the heat treatment with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, activating the second impurity.

3. (Original) The method according to claim 1, wherein the first impurity is ion-implanted to the surface layer of the semiconductor substrate at concentration of 1×10^{19} cm^{-3} or more.

4. (Previously Presented) The method according to claim 1, wherein at least one of group IV-A elements is used as the first impurity.

5. (Currently Amended) The method according to claim 1, further comprising:

pre-heating the semiconductor substrate to a predetermined temperature of 600°C or less before the heat treatment is carried out with respect thereto; and

carrying out the heat treatment with respect to the semiconductor substrate after the pre-heating is made, the heat treatment being flash lamp annealing carried out under conditions that a light emitting time is 100 msec or less and an irradiation energy density is 100 J/cm^2 or less.

6. (Canceled)

7. (Currently Amended) The method according to claim 5, further comprising:

carrying out said pre-heating to the semiconductor substrate using at least one of a hot plate, a heating lamp, and laser beams.

8. (Currently Amended) The method according to claim 7, further comprising:

using any of a hydrogen lamp, a xenon lamp, and a halogen lamp as the heating lamp.

9. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

providing a gate electrode having a gate insulating film on one side of a semiconductor substrate;

implanting an electrically inactive first impurity over substantially the entire side of the semiconductor substrate provided with the gate electrode, excluding a region below the gate electrode, to form an implanted layer on an upper portion of the gate electrode and a surface layer of the semiconductor substrate, and implanting an electrically active second impurity having a predetermined conduction type to the semiconductor substrate to a region adjacent to the gate electrode of the semiconductor substrate using the gate electrode as a mask;

forming shallow source/drain diffusion regions having the predetermined conduction type, the shallow source/drain diffusion regions being formed in a manner such that a heating treatment using light carried out on the semiconductor substrate implanted with the first and second impurities activates the second impurity,

providing a gate sidewall film on the side of the semiconductor substrate around the gate electrode;

implanting the first impurity to the side of the semiconductor substrate, excluding a region below the gate electrode, and implanting the second impurity on the

semiconductor substrate in a region adjacent to the gate sidewall film of the semiconductor substrate using the gate electrode and the gate sidewall film as a mask; and

forming deep source/drain diffusion regions having the predetermined conduction type, and continuing with the shallow source/drain diffusion regions, the deep source/drain diffusion regions being formed in a manner such that the heating treatment carried out on the semiconductor substrate implanted with the first and second impurities activates the second impurity,

wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, an upper portion of an isolation region formed in the surface layer of the semiconductor substrate, and an upper portion of the gate sidewall film.

10. (Original) The method according to claim 9, wherein the first impurity is ion-implanted to the surface layer of the semiconductor substrate at concentration of 1×10^{19} cm^{-3} or more.

11. (Previously Presented) The method according to claim 9, wherein at least one of group IV-A elements is used as the first impurity.

12. (Currently Amended) The method according to claim 9, further comprising:

pre-heating the semiconductor substrate to predetermined temperature of 600°C or less before the heat treatment is carried out with respect thereto; and

carrying out the heat treatment with respect to the semiconductor substrate after the pre-heating is made, the heat treatment being flash lamp annealing carried out under conditions that a light emitting time is 100 msec or less and an irradiation energy density is 100 J/cm^2 or less.

13. (Canceled)

14. (Currently Amended) The method according to claim 12, further comprising:

carrying out said pre-heating to the semiconductor substrate using at least one of a hot plate, a heating lamp, and laser beams.

15. (Currently Amended) The method according to claim 14, further comprising:

using any of a hydrogen lamp, a xenon lamp, and a halogen lamp as the heating lamp.

16. (Withdrawn) A semiconductor device comprising:

a semiconductor substrate subjected to heat treatment using light after electrically inactive first impurity is entirely implanted.

17. (Withdrawn) The device according to claim 16, further comprising:

the semiconductor substrate to which electrically active second impurity having predetermined conduction type is implanted, and the semiconductor substrate being

subjected to the heat treatment so that the second impurity is activated after the first and second impurities are implanted.

18. (Withdrawn) The device according to claim 16, wherein the first impurity is ion-implanted to the surface layer of the semiconductor substrate at concentration of 1×10^{19} cm^{-3} or more.

19. (Withdrawn) The device according to claim 16, wherein at least one of group IV-B elements is sued as the first impurity.

20. (Withdrawn) The device according to claim 19, wherein at least one of C, Si, Ge, Sn and Pb is used as the first impurity.

21. (Withdrawn) A semiconductor device comprising:

a semiconductor substrate formed with source/drain diffusion regions having predetermined conduction type, the semiconductor substrate being subjected to the following treatment such that electrically inactive first impurity is entirely implanted to the semiconductor substrate while electrically active second impurity having predetermined conduction type being implanted thereto, and the source/drain diffusion regions being formed in a manner that heating treatment using light is carried out the semiconductor substrate to which the first and second impurities are implanted, and thereby, the second impurity is activated; and

a gate electrode provided on the source/drain diffusion regions, and having a gate insulating film and a gate sidewall film.

22. (Withdrawn) The device according to claim 21, wherein the first impurity is ion-implanted to the surface layer of the semiconductor substrate at concentration of 1×10^{19} cm^{-3} or more.

23. (Withdrawn) The device according to claim 21 wherein at least one of group IV-B elements is sued as the first impurity.

24. (Withdrawn) The device according to claim 23, wherein at least one of C, Si, Ge, Sn and Pb is used as the first impurity.

25. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

implanting at least one of a group IV–A element as an electrically inactive first impurity over substantially one entire side of a semiconductor substrate, to form an implanted layer on a surface layer of the semiconductor substrate; and

carrying out a heat treatment using light on the one side of the semiconductor substrate implanted with the first impurity, the light having a main spectrum in a range of wavelength shorter than a silicon (Si) absorption end, and an emitting time of the light being 100 msec or less.

wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including a gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate.

26. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

providing a gate electrode having a gate insulating film on one main surface of a semiconductor substrate;

implanting at least one of a group IV–A element as an electrically inactive first impurity over substantially an entire side of the semiconductor substrate provided with the gate electrode, excluding a region below the gate electrode, to form an implanted layer on an upper portion of the gate electrode and a surface layer of the semiconductor substrate, and implanting an electrically active second impurity having a predetermined conduction type on the semiconductor substrate in a region adjacent to the gate electrode of the semiconductor substrate using the gate electrode as a mask;

forming shallow source/drain diffusion regions having the predetermined conduction type, the shallow source/drain diffusion regions being formed in a manner such that a heating treatment using light carried out on the semiconductor substrate implanted with the first and second impurities activates the second impurity, the light having a main spectrum in a range of wavelength shorter than a silicon (Si) absorption end, and an emitting time of the light being 100 msec or less;

providing a gate sidewall film on the side of the semiconductor substrate around the gate electrode;

implanting the first impurity to the side of the semiconductor substrate, excluding a region below the gate electrode and the gate sidewall film, and implanting the second impurity on the semiconductor substrate in a region adjacent to the gate sidewall film of the semiconductor substrate using the gate electrode and the gate sidewall film as a mask; and

forming deep source/drain diffusion regions having the predetermined conduction type, and continuing with the shallow source/drain diffusion regions, the deep source/drain diffusion regions being formed in a manner such that the heating treatment using the light carried out on the semiconductor substrate implanted with the first and second impurities activates the second impurity,

wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, an upper portion of an isolation region formed in the surface layer of the semiconductor substrate, and an upper portion of the gate sidewall film.

27. (Currently Amended) The method according to claim 1, wherein the one entire side includes [[a]] the semiconductor element forming region and [[an]] the isolation region.

28. (Currently Amended) The method according to claim 9, wherein the entire side includes [[a]] the semiconductor element forming region and [[an]] the isolation region.

29. (Currently Amended) The method according to claim 25, wherein the first and second impurities are implanted to the one entire side having [[a]] the semiconductor element forming region and [[an]] the isolation region of the semiconductor substrate.

30. (Previously Presented) The method according to claim 26, wherein the first and second impurities are implanted to the entire side having a semiconductor element forming region and an isolation region of the semiconductor substrate.

31. (New) The method according to claim 1, wherein the first impurity is implanted to an nMOS region and a pMOS region.

32. (New) The method according to claim 9, wherein the first impurity is implanted to an nMOS region and a pMOS region.

33. (New) The method according to claim 25, wherein the first impurity is implanted to an nMOS region and a pMOS region.

34. (New) The method according to claim 26, wherein the first impurity is implanted to an nMOS region and a pMOS region.